module p3(out, zero\_flag, alu1, alu2, data\_in, clk, write\_enable, selA, selB, selD, selOP);

output reg[7:0] out, alu1, alu2;

output reg zero\_flag;

input clk, write\_enable;

input[7:0] data\_in;

input[2:0] selA, selB, selD, selOP;

reg [7:1] register[7:0];

initial

begin

register[1]=8'h00;

register[2]=8'h00;

register[3]=8'h00;

register[4]=8'h00;

register[5]=8'h00;

register[6]=8'h00;

register[7]=8'h00;

end

always @(posedge clk)

begin

if(selA==0)

alu1 <=data\_in;

else

alu1 <=register[selA];

if(selB==0)

alu2 <=data\_in;

else

alu2 <=register[selB];

case(selOP)

3'b000 : out=alu1+alu2;

3'b001 : out=alu1-alu2;

3'b010 : out=alu1\*alu2;

3'b011 : out=alu1/alu2;

3'b100 : out=alu1&alu2;

3'b101 : out=alu1|alu2;

3'b110 : out=alu1^alu2;

3'b111 : out=alu1;

endcase

if(write\_enable && selD!==0)

register[selD]<=out;

if(out==0)

zero\_flag <=1;

else

zero\_flag <=0;

end

endmodule

module tb\_p3();

wire[7:0] out, alu1, alu2;

wire zero\_flag;

reg[7:0] data\_in;

reg clk, write\_enable;

reg[2:0] selA, selB, selD, selOP;

integer i;

initial

begin

clk=1;

write\_enable=1'b1;

data\_in=$urandom%2\*\*8;

selA =3'b000;

selB =3'b111;

selD =3'b000;

selOP=3'b111;

#10;

for (i=0; i<=15; i=i+1)

begin

data\_in=$urandom%2\*\*8;

selA =$urandom%2\*\*3;

selB =$urandom%2\*\*3;

selD =$urandom%2\*\*3;

selOP=$urandom%2\*\*3;

#10;

end

end

always #5 clk=~clk;

p3 UUT(out, zero\_flag, alu1, alu2, data\_in, clk, write\_enable, selA, selB, selD, selOP);

endmodule

